9th December 1965 BG

A STOCHASTIC [redacted] COMPUTER

Some Notes on the Application of Digital Circuits to the Operations of Arithmetic and Differential Calculus by Means of a Probabilistic Representation of Quantities

Introduction Conventional digital computers are devices for implementing logical calculations. Conventional analog computers are devices for implementing arithmetical calculations. When the former is used to simulate the latter, numbers are stored as complexes of binary events and operations such as multiplication and addition are carried out by a complex, logical central processor. The analog computer has the advantage that its operations are carried out in parallel but the disadvantages that they are on a uniform time-scale and are implemented by components which have to be very precise and (when storage is required) very large. The digital computer has the advantage that its components are small and (being two state) imprecise, but the disadvantage that its processing is sequential and parallel operation is practically impossible.

It is proposed here that digital techniques may be used to handle and process analog data more directly if the analog quantities are represented not as voltage levels, nor as multiple binary events but rather as the probability that a binary event will occur (or more generally as the probability that one configuration of a multi-valued event will occur - ternary logic is especially attractive here).

It will be demonstrated that the arithmetical operations of: addition (subtraction), inversion, multiplication and integration, the normal complement of an analog computer, can readily be carried out by simple logic-circuitry which is readily realized in hardware (particularly in micro-circuits).

Stochastic analog computers have these advantages:

1. Compactness through the use of digital micro-circuits
2. High tolerance for component variation through the use of logical rather than arithmetical calculation.
3. A precision not less than that of conventional analog computers (there is a precision/bandwidth product similar to conventional gain/bandwidth products)
4. Parallel operation through the use of independent elements.
5. Indeterminate time-scale operation - it is possible for one section of the computer to control the time-scale of another making it feasible to study partial differential

equations directly rather than by iteration.

6.Ease of implementation of adaptive schemes through the ready availability of multiplier and storage circuitry(adjustable coefficients).

The disadvantage of the stochastic analog computer is that its bandwidth is restricted by the number of events needed to define accurately a probability. For example, to determine the probability that a binary device will be on with less than 1% probability of being more than 1% out requires 20,000 observations. Since the probability has to be essentially constant over this period the clock rate of the digital logic must be divided by a factor of this order of magnitude to calculate the resultant bandwidth of the stochastic analog computer eg.100 cs bandwidth requires at least 2Mcs logic (this itself must be multiplied by a factor, at present 100 but possibly considerably less, to obtain the upper limit required of the digital logic required to generate probabilities during clock pulses).

Representation of Quantities by Probabilities In the conventional analog computer quantities are represented by voltages in a given range from zero up (asymmetric or single-quadrant) or centred about zero (symmetric or four-quadrant), and all quantities must be scaled to lie within the range of the computer. Similarly in the stochastic analog computer quantities must be scaled to lie within a given range which may be taken without loss of generality to be zero to plus one in the asymmetric case and zero plus or minus one in the symmetric case. To map voltages from zero to one onto probabilities in the same range we may take:

$$p(on) = V \qquad 0 \leq V \leq 1$$

and similarly for voltages centred about zero:

$$p(on) = (1+V)/2 \qquad -1 \leq V \leq +1$$

In the latter situation zero voltage is represented by a probability of one half.

Both these scales are of interest but the latter is more powerful and of main importance.

Synchronous logic systems The basic elements of a synchronous logic system are boxes with input and output lines plus a clock pulse line. The input lines are connected to the output lines of other boxes and have the logic levels on or off applied to them. The output lines are at logic levels on or off according to the state of the box. When a clock pulse is applied the outputs and state take new values dependent upon the inputs

and the state. It is this logic configuration that will be considered for the stochastic computer and analog variables will be represented by probabilities of states, inputs and outputs. Other forms of logic may be considered and asynchronous frequency (mean pulse rate) or mark-space (with random frequency) might be used. These lead to complications in the theory and to the major disadvantage that the time-scale of the logic is then fixed. Much power may be gained with synchronous logic by considering configurations where the clock pulse to a part of the system is itself a random variable.

Stochastic Multiplication and Isolation In a conventional analog computer multiplication is the most exacting operation and in the digital computer it requires a great deal of time and hardware. However in the stochastic analog computer it is a simple logical operation with minimal circuitry. Consider two idependent events with probabilities p and r, then the probability of their joint occurrence is pr. Thus for asymmetric multiplication a single 'and' gate suffices (Fig.1.). Similarly the more complex 'equality' gate (implementing the function $a.b \wedge \bar{a}.\bar{b}$) is sufficient for symmetric or four-quadrant multiplication (Fig.2.)

One of the crucial problems of stochastic logic appears when it is desired to use the above circuitry as a squarer. It is not sufficient to common the input lines since the inputs will not then be statistically independent and in fact the input will pass through unchanged. However a statistically independent replication of a line may be obtained by delaying it through one clock pulse. Thus a delay acts as a statistical isolator (Fig.3.) and can be used in conjunction with a multiplier to provide squaring (Fig.4.) or higher powers. The use of a delay in this way is important whenever a signal takes multiple paths and care must be taken in computer configurations to avoid artifacts due to lack of statistical idependence. These can always be obviated by suitable isolation.

Stochastic Inversion Both symmetric and assymmetric inversion are realised by a logical invertor.

Stochastic Addition The operations so far have been implemented with simple logical elements and it is reasonable to suppose that addition can be realized in a similar way. However the simple 'or' gate fails since it yields not the sum of the input lines but their sum minus their product; this defect occurs because only one output occurs for inputs on both lines. In fact deterministic logic is unable to implement the required operation and stochastic logic is required instead. To sum a number of lines the adder chooses one of them at random and outputs the value of that line. Thus the output of a k-input adder is $1/k$ times the sum of its inputs. Circuitry is shown in Fig.7. where the counter enables one of the input lines at random choosing each one with equal probability. There is no difference

between symmetric and asymmetric adders.

Generation of Random Sequences The stochastic adder has within it a random element and may generate random sequences even when its inputs are deterministic. In general, however, the random sequences which carry information in a stochastic computer will be generated either internally as the output of stochastic constants and integrators or externally from the conversion of analog or digital numbers into a stochastically coded form. The element which does this is a comparator with binary output, one of whose inputs is random or pseudo-random and the other of which is fixed (stochastic constant) or from external world (stochastic conversion at interface) or integrator state (see later section). The only requirement on inputs to the comparator is that it should be possible to say which one is greater in magnitude and thus two voltages or two digitally coded numbers or even two pressures might be used. The random input is generally required to take all its possible levels with equal probability (though specific random distributions may be very useful for nonlinear conversion) and this may be achieved by random selection of its levels as was done in the adder (Fig.6.). Since the number of levels will generally be much greater than were the number of inputs to an adder, it is preferable to generator the random states of the binary counter not by cycling but by randomly changing every bistable - this enables much faster random generation.

Stochastic Integration The natural element to use for integration is a reversible binary counter incrementing on a clock pulse if its input is on and decrementing otherwise. Whilst this is all that can be done if the integrator has a single input it may be shown that this is not the optimum configuration if the integrator is used with a two-input adder (a very common configuration since integrators generally have feedback around them). When there are two inputs the binary counter should increment when they are both on, decrement when they are both off and remain in the same state if one is on and the other is off. Thus the basic component is best thought of as a two-input summing integrator and realized (Fig.7.) by a reversible binary counter with end-stops (so that it does not increment from its maximum level to its minimum or vica versa). The output of the integrator is a random sequence generated in the manner described above.

When only one input is fed to the integrator both its input terminals may be commoned, preferably in conjunction with an isolator as shown in Fig.8. If the output of the integrator is fed back to one of its inputs then the configuration is an ADDIE and the state of the integrator estimates the

probability of an input. Thus the ADDIE is a suitable output interface for the stochastic computer. The time constant of the integrator is proprtional to the number of states of the binary counter (equivalent to the size of capacitor in a conventional integrator) and this can be varied within the integrator by changing the end-stops and the random generator (which of course varies between the end stops); this is called the 'age' in an ADDIE.

Interface The stochastic computer may have no inputs from the external world (in solution of differential equations) or may receive analog inputs which are converted into random sequences as previously decribed or digital inputs which may be converted into random sequences or may be used to set the state of an integrator. This latter is very important since an integrator used without inputs can hold a constant and hence is a convenient way of setting the computer parameters externally.

Integrators are the natural outward interface of the stochastic computer since the binary counter may be read out as such or used to set an analog level. If there are integrators within the computer these form useful read-out points otherwise an integrator which is re-set once every time-constant (moving average) or an ADDIE (exponential smoothing) may be used.

Thus the stochastic computer is readily used in conjuction with conventional analog and digital womputers, and as a part of information processing systems where the data is carried in some other form.

Patent Application The novelty of the stochastic computer does not lie in the basic elements which are conventional digital circuits but rather in the combination of these circuits for the purpose of calculation. One way of regarding the circuits described is as accessories to the basic ADDIE already patented. These devices allow the ADDIE to be used as a multiplier, a squarer, an adder etc. and allow differential operators to be interpolated with the ADDIE. Thus the power of the ADDIE is greatly increased because a complete family of stochastic elements is available which can be used to perform a wide range of calculations; the full power of the stochastic output of the ADDIE cannot be utilized without these additional elements.

In Fig.9. etc. are shown configurations of the elements described above so as to make complete functional units. These units show the use of each element on its own and in conjunction with others, and provide a full illustration of the stochastic computer.

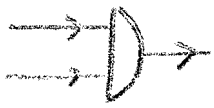


FIG 1

ASYNCHRONOUS MULTIPLEXER

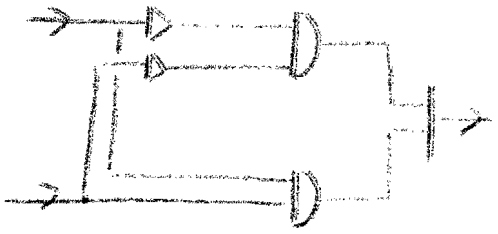
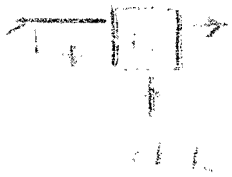


FIG 2

SYNCHRONOUS MULTIPLEXER



FIG

DEMUX

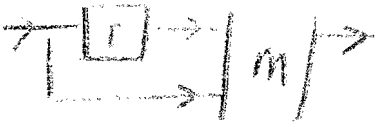


FIG 4

SCRAMBLER

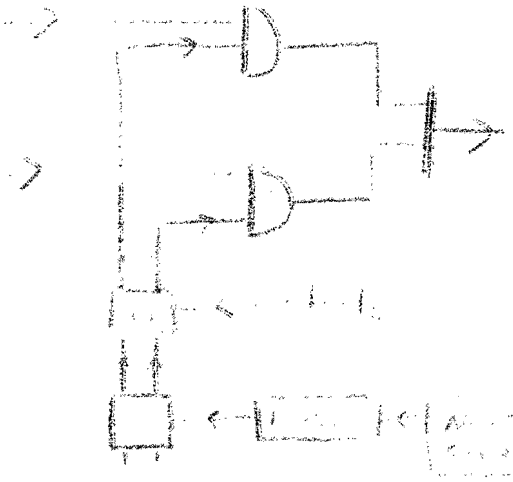
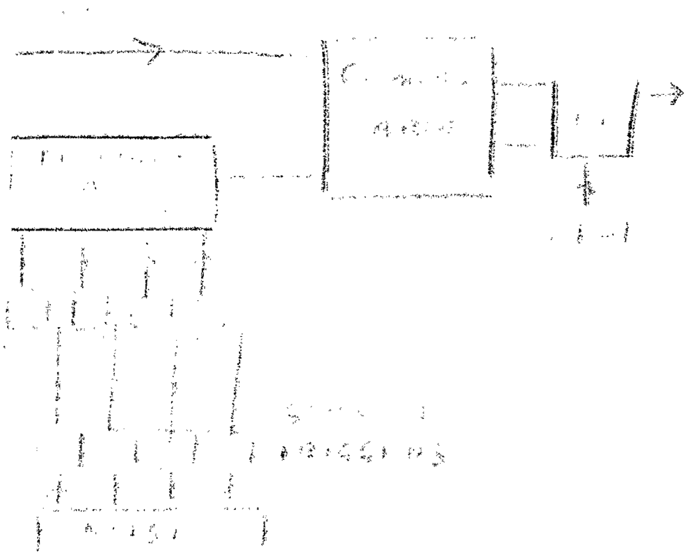
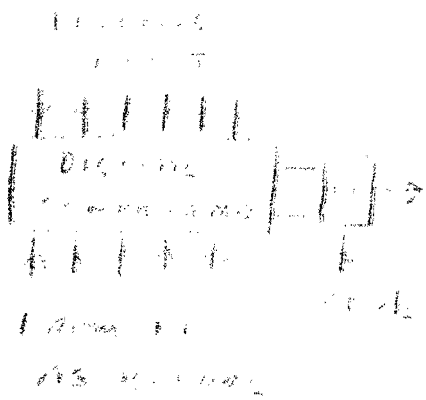


FIG 5

TWO INPUT ADDER

The basic flip flop is a master slave which is triggered on the upper edge of a clock pulse. The upper AND selects the channel according to the output





ANALOG STOCHASTIC CONVERTER — FIG 6 — DIGITAL STOCHASTIC CONVERTER

There will normally be more than 4 [illegible] ([illegible]) in the digital noise generator. These are in a random state at times giving a random level to the comparator. If at a clock pulse the analog or digital input is greater than the random input then the output flip flop goes on.

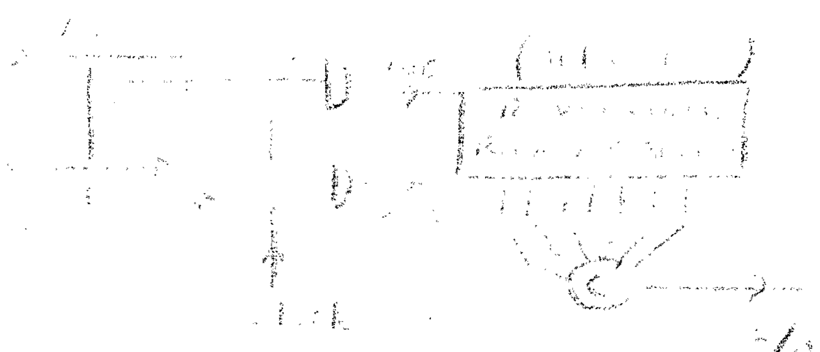


FIG 6

Two [illegible]

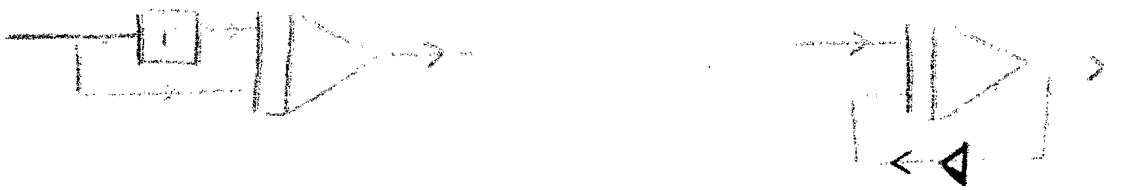
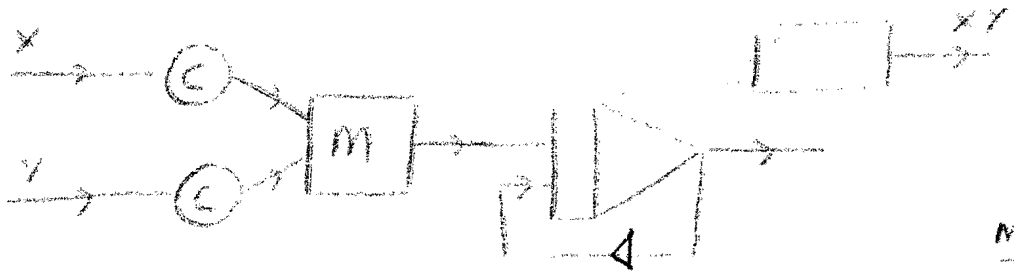
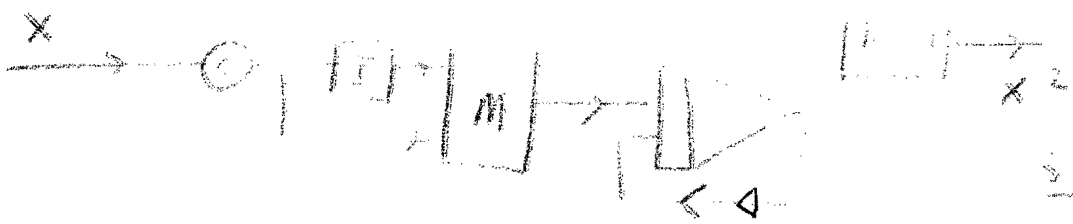


FIG 5





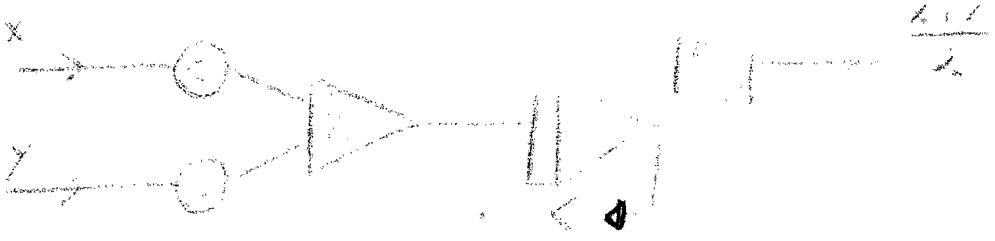


FIG 9

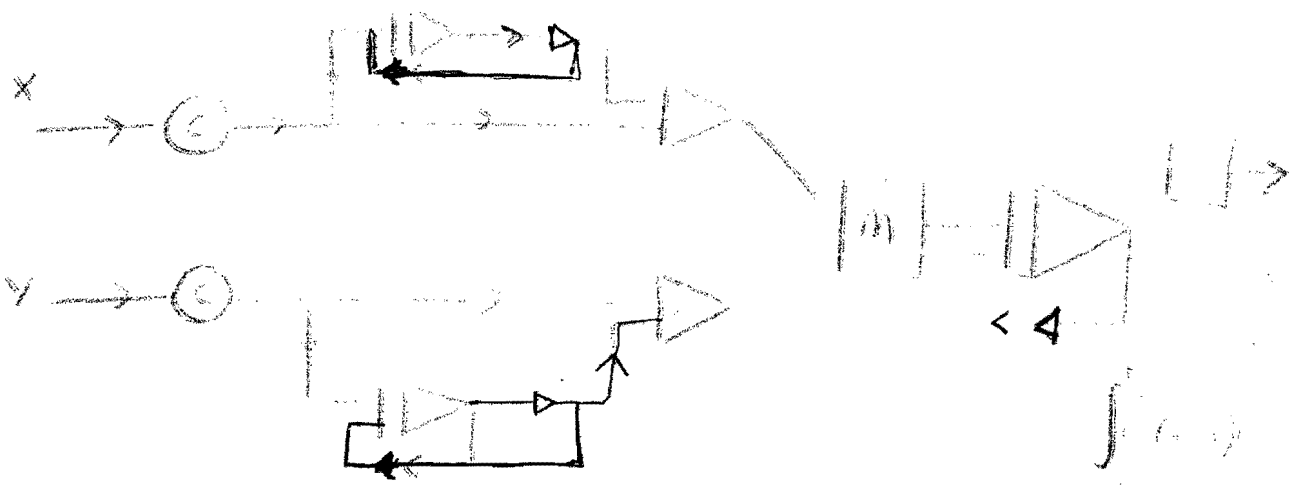
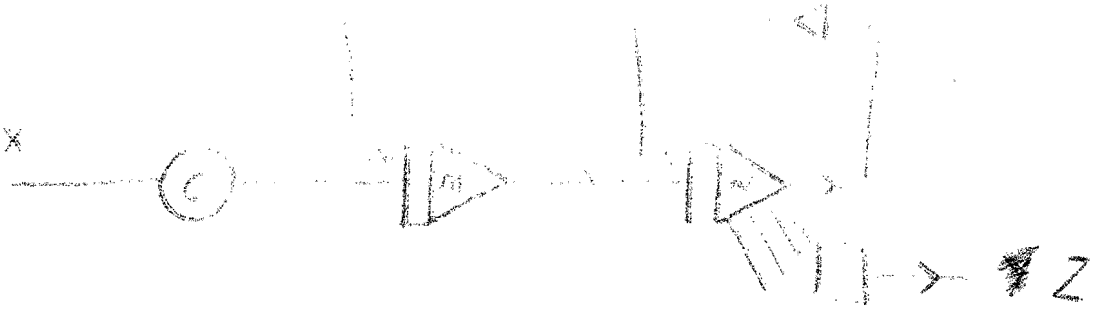


FIG 10

Cross-Correlation $Cov(x,y)$



$$Z + \frac{1}{N} \dot{Z} + \frac{1}{m\omega} Z = \frac{x}{m\omega}$$

FIG 11

$\omega^2 = \frac{1}{mN}$

$2J = \sqrt{\frac{m}{N}}$

SYMBOLS